Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 17 as with the following amended paragraph:

The pixels 913 each have a switching transistor 915, and **[[an]]** a SRAM 916 having a plurality of transistors. A gate electrode of the switching transistor 915 is connected to the scanning line 917. Further, one of a source region and a drain region of the switching transistor 915 is connected to the data line 918, and the other is connected to an input terminal Vin of the SRAM 916 and to the first address electrode 902a.

Please replace the paragraph beginning at page 9, line 25 as with the following amended paragraph:

each one of the plurality of pixels has a switching transistor, **[[an]]** a SRAM, a transistor for the erasing operation, a first address electrode and a second address electrode;

Please replace the paragraph beginning at page 11, line 9 as with the following amended paragraph:

each one of the plurality of pixels has a switching transistor, **[[an]]** a SRAM, a transistor for the erasing operation, a first address electrode and a second address electrode;

Please replace the paragraph beginning at page 13, line 17 as with the following amended paragraph:

each of the plurality of pixels has a first switching transistor, a second switching transistor, **[[an]]** a SRAM, a first address electrode, and a second address electrode;

Please replace the paragraph beginning at page 14, line 1 as with the following amended paragraph:

each of the plurality of pixels has a first switching transistor, a second switching transistor, **[[an]]** a SRAM, a first address electrode, and a second address electrode;

Please replace the paragraph beginning at page 14, line 22 as with the following amended paragraph:

each of the plurality of pixels has a first switching transistor, a second switching transistor, **[[an]]** a SRAM, a first address electrode, and a second address electrode;

Please replace the paragraph beginning at page 15, line 18 as with the following amended paragraph:

each of the plurality of pixels has a first switching transistor, a second switching transistor, **[[an]]** a SRAM, a first address electrode, and a second address electrode;

Please replace the paragraph beginning at page 18, line 13 as with the following amended paragraph:

Fig. 16 is an equivalent circuit diagram of **[[an]]** a SRAM;

Please replace the paragraph beginning at page 19, line 16 as with the following amended paragraph:

The pixel 113 has a switching transistor 115a and erasure transistor 115b, and **[[an]]** a SRAM 116 having a plurality of transistors. A gate electrode of the switching transistor115a is connected to the write in scanning line 117a. Further, a gate electrode of the erasure transistor 115b is connected to the erasure scanning line 117b.

Please replace the paragraph beginning at page 48, line 25 as with the following amended paragraph:

A structure of **[[an]]** a SRAM used in the present invention is explained in embodiment 9.

Please replace the paragraph beginning at page 48, line 27 as with the following amended paragraph:

Fig. 16 shows an example of a circuit diagram of **[[an]]** a SRAM. The SRAM has two each of p-channel transistors and n-channel transistors. Source regions of each of the p-channel transistors are connected to the high voltage side electric power source Vddh, while source regions of each of the n-channel transistors are connected to the low voltage side electric power source Vss. One p-channel transistor and one n-channel transistor form a pair, and two sets of the p-channel transistor and n-channel transistor pairs exist within one SRAM.

Please replace the paragraph beginning at page 49, line 12 as with the following amended paragraph:

A structure of **[[an]]** a SRAM used by the present invention and having a structure which differs from that of Fig. 16 is explained next.

Please replace the paragraph beginning at page 49, line 14 as with the following amended paragraph:

Fig. 17A shows an equivalent circuit diagram of **[[an]]** a SRAM of embodiment 9. The SRAM has two p-channel transistors and two resistors. One p-channel transistor and one resistor become a pair, and two sets of p-channel transistor and resistor pairs exist within one SRAM. The source region of the p-channel transistor is connected to the high voltage side electric power source Vddh, and the drain region is connected to the low voltage side electric power source Vss through the resistor.

Please replace the paragraph beginning at page 49, line 34 as with the following amended paragraph:

Fig. 17B shows an equivalent circuit diagram of **[[an]]** a SRAM of embodiment 9. The SRAM has two n-channel transistors and two resistors. One n-channel transistor and one resistor

become a pair, and two sets of n-channel transistor and resistor pairs exist within one SRAM. The drain region of the n-channel transistor is connected to the high voltage side electric power source Vddh, and the source region is connected to the low voltage side electric power source Vss through the resistor.